Aloha Proof Module System Testing
Standards and Procedures

In order to devise a testing plan for Proof Module we should first define and specify the functionality of the Proof Module. This consists of five areas: 1) power supply, 2) hydrophone, 3) DigiQuartz pressure sensor, 4) microcontroller, and 5) digital communications. Since all the data (hydrophone audio stream, power supply voltages and currents, DigiQuartz pressure, temperatures, etc.) are multiplexed into a single data stream, there is only one major issue and that is the integrity of the data communications and any data error bit error rate (BER). The Proof Module is being operated on the bench around the clock and is being continually monitored for system functionality. This includes both computer analysis and human observations (listening to the audio).

1) Power Supply: Since the power supply is a nominal 20 watt supply and is fully heat sinked to the pressure case, the heat is negligible. The proof module has been operation for over four months on the bench on the power supply. The voltages and currents are monitored by the microcontroller at three second intervals and passed on as engineering data stream.
2) Hydrophone: the audio input is operating with a substitute audio signal and is operation continuously around the clock. The audio is being digitized at 96,000 samples per second, Manchester encoded, and sent over the AT&T communication equipment (on the bench).
3) DigiQuartz pressure sensor: this data is sampled by the microcontroller and passed on in the engineering data stream.
4) The microcontroller is monitors temperatures in addition to the signals above. It processes and formats all the engineering data and send it as RS232 data to the Manchester encoder. The Manchester encoder embeds this into the 64 bit frame of the audio stream.
5) Digital serial communications: Since all the data is multiplex into one data stream, this test procedure will thoroughly test the data communications.

Test Procedure for Proof Module Communcaion System:

The test procedure for the Proof Module will be the substitution of the digitized audio signal with a specialized pseudorandom digital stream directly into the input of the Manchester encoder and then a real time computer analysis of this data stream at the Manchester decoder and de-multiplexer at the receive end. It will be fully checked for any bit error in the transmission over all the steps of the process, including Manchester, MULDEX, AT&T repeaters, fiber optic cables, etc. This is a full BER test.

Method**:**

Transmission: A specialized circuit will be board will be produced that will produce a 32 bit pseudorandom data stream in a 32 bit shift register. Those 32 bits will be shifted into a second 32 bit shift register, but will be inverted to contain the complement. As these 64 bit are being streamed this circuit will frame them into the format of the ADC converter. This will involve 1) the left/right frame clock, 2) the left channel will be 24 bits of the pseudorandom stream with 8 bits nulled (required in format), and 3) the right channel will be 24 bits of complemented pseudorandom stream with 8 bits nulled.

Analysis: A computer with the receiving hardware PCI board will analyze each frame. The 24 bits of the left channel be compared to the 24 bits of the right channel after it has been re-inverted back to the original value. Every frame and each of the 48 bits (2 x 24) will be checked. Should one or more bit errors occur, it will be counted and compared to the total bit count**.**

Definition of Error: Since the nth bit of the left channel is compared to the complemented nth bit of the right channel. If they do not compare, an error is determined. This is done for all 24 bits and for every frame.

Limitations: Although all errors will be detected, it will not be able to identify specifically the location of the bit. Since the nth bit of both channels are compared to each other (and not to an absolute standard), it will not be able to determine if the error is in the left channel bit error position or the right channel bit error position, but only that one or the other was in error. Thus, for any error, if any, there will be two possibilities**.**

Calculations of bit error rate: Although the frames are 64 bits they will not be counted as 64 bits. Because the data actually is 24 bit per channel and because it takes comparing one bit from each channel to determine one error, the most possible errors per frame is 24 (assuming ever bit is wrong). Therefore, the BER rate will be determined as the number of error bits divided by the number of frames times 24.

BER = (Error Bit Counts) / (Frame Counts x24)

Schematics: The schematic of the pseudorandom digital stream generator and the PLD logic are in the two PDF files _____ and _____.