```
/*  IRIG_WD2.TDL   PAL U10 FOR ALOHA OBSERVATORY IRIG TIME CONTROL VERSION 1*/
#define JEDFILE  "IRIG_WD2.JED"
#define DESIGNER James Jolly
#define  COMPANY SOEST Design and Engineering Group
#define  PARTNUM PEEL22V10   (P22V10, board refdes: Uxx)
#define REVISION 1.00  (Last change:  19 JUly 2004)
#define COMMENTS \
                                                \
        Includes TEST VECTORS.

/*
 *
 */

palname (in DUMMY1,                 /* com reg clock */
        RXAA,    RXAB,              /* inputs */
        STRBWDA, STRBWDB,
        WDENA,   WDENB,
        RESA_,   RESB_,
        WDRESA_,
        RESTA_,  RESTB_;
    io  WDRESB_,  DUMMY2,            /* I/O outputs */
        INHA_,   INHB_,
        POR_,    POR,
        WDCLRA,  WDCLRB,
        RESETA_, RESETB_)

{

   INHA_.oe  = INHB_.oe = WDRESB_.oe = DUMMY2.oe = 0;
   WDCLRA.oe =  POR_.oe = RESETA_.oe = 1;
   WDCLRB.oe =  POR.oe  = RESETB_.oe = 1;

/*      EQUATIONS:      */

     POR_    = (RESA_ & RESB_) | !INHA_ | !INHB_;
     POR     = !POR_;

     WDCLRA  = (RXAA & !STRBWDA) | (!RXAA & STRBWDA); /* exclusive OR */
     WDCLRB  = (RXAB & !STRBWDB) | (!RXAB & STRBWDB); /* exclusive OR */

    !RESETA_ = (!WDRESA_ & WDENA) | !RESTA_;
    !RESETB_ = (!WDRESB_ & WDENB) | !RESTB_;

    putpart("P22V10", JEDFILE ,
     DUMMY1, RXAA,  RXAB, STRBWDA, STRBWDB, WDENA, WDENB, RESA_, RESB_, WDRESA_,
RESTA_,  GND,
     RESTB_, WDRESB_, DUMMY2,  WDCLRB,  POR_,    POR,   INHA_, INHB_, WDCLRA,
RESETA_, RESETB_, VCC);

}
```