```
/*  IRIG_CT1.TDL   PAL U11 FOR ALOHA OBSERVATORY IRIG CONTROL VERSION 1*/
#define JEDFILE  "IRIG_CT1.JED"
#define DESIGNER James Jolly
#define  COMPANY SOEST Design and Engineering Group
#define  PARTNUM PEEL22V10   (P22V10, board refdes: Uxx)
#define REVISION 1.00  (Last change:  19 May 2004)
#define COMMENTS \
                                                \
        Includes TEST VECTORS.

/*
 *
 */

palname (in TAKE,             /* com reg clock */
        WDRES_,               /* inputs */
        IORD_,   LOAD1_, LOAD2_,
        TAKEA,   TAKEB,
        ENAPPS,  ENBPPS,
        DUMMY1,  DUMMY2,
        DUMMY3;
    reg R_LCLA_;               /* I/O outputs */
    io  LCLB_,  DUMMY7,
        AEN,    PPS1RUN,
        DIR,
        DUMMY9, DUMMY10, DUMMY11,
        TAKEOUT)

{
  R_LCLA_.ck =   TAKE;
  R_LCLA_.pre =  0;
  R_LCLA_.aclr = !WDRES_;

   DUMMY7.oe  = PPS1RUN.oe  = DUMMY9.oe  = DUMMY10.oe   = DUMMY11.oe = 1;
   R_LCLA_.oe = LCLB_.oe = AEN.oe = DIR.oe  = TAKEOUT.oe = 1;

/*      EQUATIONS:      */

    AEN     = 0;

    DIR     =  IORD_ & LOAD1_ & LOAD2_; /* qualified RMT_  for SDI on ADC
chips*/

    PPS1RUN = ENAPPS & ENBPPS;

    TAKEOUT = (TAKEA & !TAKEB) | (!TAKEA & TAKEB);  /* exclusive OR */

    R_LCLA_ = LCLB_;

      LCLB_ = !R_LCLA_;

    putpart("P22V10", JEDFILE ,
     TAKE,   WDRES_,  IORD_, LOAD1_, TAKEA, TAKEB,   ENAPPS, ENBPPS, LOAD2_,
DUMMY1,  DUMMY2,  GND,
     DUMMY3, R_LCLA_, LCLB_, DUMMY7, AEN,   PPS1RUN, DIR,    DUMMY9, DUMMY10,
DUMMY11, TAKEOUT, VCC);
```

```
}
```