```
/*      PAL U7 FOR ALOHA OBSERVATORY USER ENDCAP CONTROL VERSION 3*/
#define JEDFILE  "CTRL_UE3.JED"
#define DESIGNER James Jolly
#define  COMPANY SOEST Design and Engineering Group
#define  PARTNUM PEEL22V10   (P22V10, board refdes: Uxx)
#define REVISION 1.00  (Last change:  19 May 2004)
#define COMMENTS \
                                                \
        Includes TEST VECTORS.

/*
 *
 */

palname (in RXA,              /* com reg clock */
        RCPOR,                /* inputs */
        WDENA,    WDOUT_,
        RES_,     RLCL_,
        STRBWD,   DUMMY1,
        DUMMY2,   CS1,
        CS2,      RESET;
    reg R_SMOD;               /* I/O outputs */
    io  CS1_,     CS2_,
        RMT_,     POR_,
        ISORMT_,
        QLCL_,    QRMT_,
        WDCLR,    RESET_)

{
   R_SMOD.ck =   RXA;
   R_SMOD.pre =  0;
   R_SMOD.aclr = !RCPOR;

   CS1_.oe    = CS2_.oe  = RMT_.oe  = POR_.oe   = R_SMOD.oe = 1;
   ISORMT_.oe = QRMT_.oe = QLCL_.oe = WDCLR.oe  = RESET_.oe = 1;


/*      EQUATIONS:      */

   !RMT_    = RLCL_;

   !ISORMT_ = RMT_;

   !CS1_    = CS1;

   !CS2_    = CS2;

    POR_    = RES_;

    QLCL_   = (CS1_ & CS2_) | RLCL_;  /* qualified RLCL_ for SDI on ADC chips*/

    QRMT_   = (CS1_ & CS2_) | RMT_;   /* qualified RMT_  for SDI on ADC chips*/

    WDCLR   = (RXA & !STRBWD) | (!RXA & STRBWD); /* exclusive OR */

    !RESET_  = (!WDOUT_ & !WDENA) | !RESET;
```

```
    R_SMOD = 1;

    putpart("P22V10", JEDFILE ,
     RXA,   RCPOR, WDENA,  WDOUT_, RES_, RLCL_,  STRBWD,  DUMMY1, DUMMY2, CS2,
CS1,    GND,
     RESET, CS2_,  CS1_,   RMT_,   POR_, R_SMOD, ISORMT_, QRMT_,  QLCL_,  WDCLR,
RESET_, VCC);

}
```