```
/*      PAL U15 FOR ALOHA OBSERVATORY POWER ENDCAP CONTROL VERSION 1*/
#define JEDFILE  "CTRL_PE1.JED"
#define DESIGNER James Jolly
#define  COMPANY SOEST Design and Engineering Group
#define  PARTNUM PEEL22V10   (P22V10, board refdes: Uxx)
#define REVISION 1.00  (Last change:  19 May 2004)
#define COMMENTS \
                                                \
        Includes TEST VECTORS.

/*
 *
 */

palname (in RXA,              /* com reg clock */
        DUMMY0,               /* inputs */
        WDENA,   WDOUT_,
        RES_,    RLCL_,
        DUMMY1,  STRBWD,
        DUMMY2,  DUMMY3,
        RCPOR,   RESET;
    reg R_SMOD;                /* I/O outputs */
    io  DUMMY5,  DUMMY6,
        RMT_,    POR_,
        ISORMT_,
        QRMT_,   QLCL_,
        WDCLR,   RESET_)

{
  R_SMOD.ck =   RXA;
  R_SMOD.pre =  0;
  R_SMOD.aclr = !RCPOR;     /* !RES_; */

   DUMMY5.oe  = DUMMY6.oe = RMT_.oe  = POR_.oe   = R_SMOD.oe = 1;
   ISORMT_.oe = QLCL_.oe  = QRMT_.oe = WDCLR.oe  = RESET_.oe = 1;

/*      EQUATIONS:      */

   !RMT_    = RLCL_;

   !ISORMT_ = RMT_;

    POR_    = RES_;

    QLCL_   =  RLCL_;  /* qualified RLCL_ for SDI on ADC chips*/

    QRMT_   =  RMT_;   /* qualified RMT_  for SDI on ADC chips*/

    WDCLR   = (RXA & !STRBWD) | (!RXA & STRBWD); /* exclusive OR */

    !RESET_ = (!WDOUT_ & !WDENA) | !RESET;

     R_SMOD = 1;

    putpart("P22V10", JEDFILE ,
     RXA,   DUMMY0, WDENA,  WDOUT_, RES_, RLCL_,  STRBWD,  DUMMY1, DUMMY2,
DUMMY3, RCPOR,  GND,
```

```
     RESET, DUMMY5, DUMMY6, RMT_,   POR_, R_SMOD, ISORMT_, QRMT_,  QLCL_,  WDCLR,
RESET_, VCC);

}
```