5	4	3		2	1
			•		· ·
UpLink Data format	(from Proof Module to C	able Station)			
Left/Right Clock					
D TT	01 00 00 10				
64 Bit Data Frame	01 00 00 10		1 10 10 10 10 10 10 10 10		
	1   0		II.	1	
	1 0	24 bit ADC left audio channel	8 bit null	24	bit ADC right audio channel
RS232 channel 1 Bit $\square$	Frame				
RS232 channel 2 Bit —	Sync				
Lock of Down Link					
Audio Overflow Bit	_				
	Engineering and Digiquartz d				
RS232 channel 2 contains the	e echo characters of the comma	nd and the responce			
c					
DownLink Data forma	t (from Cable Station t	o Proof Module)			
I					
▶ Left/Right Clock					
Left/Right Clock			•		
	10 01 00 00 10		10 10 10 10 10 10 10 10		
64 Bit Data Frame 10 10 10	0.1				
	0 1 0	RS232 channel 1 Bit (reduplicated)	10 10 10 10 10 10 10 10 10 10 10 10 10 1	RS232 char	nnel 2 Bit (reduplicated)
64 Bit Data Frame 10 10 10	0 1 0 Frame				
64 Bit Data Frame 10 10 10	0 1 0	RS232 channel 1 Bit (reduplicated) (not used)			nnel 2 Bit (reduplicated)
64 Bit Data Frame 10 10 10	0 1 0 Frame				
64 Bit Data Frame 10 10 10	0 1 0 Frame				
64 Bit Data Frame 10 10 10	0 1 0 Frame				
64 Bit Data Frame 10 10 10	0 1 0 Frame				
64 Bit Data Frame 10 10 10	0 1 0 Frame				
64 Bit Data Frame 10 10 10	0 1 0 Frame				
64 Bit Data Frame 0 0 0 0	0 1				
64 Bit Data Frame 10 10 10 0 0 0 0 Manchester Data Cel	0 1 0 Frame Sync				
64 Bit Data Frame 0 0 0 0	0 1 0 Frame Sync				
64 Bit Data Frame  10 10 10  0 0 0  Manchester Data Cel Each data cell is divided in	0 1 0 Frame Sync	(not used)			
64 Bit Data Frame  0 0 0  Manchester Data Cel Each data cell is divided in	0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	(not used)	8 bit null		
Manchester Data Cel Each data cell is divided in Each bit of the data is sen The data clock is enbedded	0 1 0 1 Frame Sync 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	(not used)  and the inversion is sent in the first half.  and in the middle of each manchester data cell	8 bit null	(Com	mand and Control)
Manchester Data Cel Each data cell is divided in Each bit of the data is sen The data clock is enbedded	0 1 0 1 Frame Sync 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	(not used)	8 bit null	(Com	mand and Control)
Manchester Data Cel Each data cell is divided in Each bit of the data is sen The data clock is enbedded	0 1 0 1 Frame Sync 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	(not used)  and the inversion is sent in the first half.  and in the middle of each manchester data cell	8 bit null	(Com	mand and Control)
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Manchester Data Cel Each data cell is divided in Each bit of the data is sen The data clock is enbedded The Frame Sync is a manches	Frame Sync  1  to two halves. t in the second half of the cell a in the data stream and is recovere ster violation because the middle	(not used)  and the inversion is sent in the first half.  and in the middle of each manchester data cell	8 bit null ation is on the first "1" imm	edeately following the v	UNIVERSITY OF HAWAII Aloha Observatory Engineering Support Facility 2525 Correa Road Honolulu, H196822
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Manchester Data Cel Each data cell is divided in Each bit of the data is sen The data clock is enbedded The Frame Sync is a mancher	Frame Sync  1  1  1  1  1  1  1  1  1  1  1  1  1	(not used)  and the inversion is sent in the first half.  and in the middle of each manchester data cell	. ation is on the first "1" imm  DATE COMM  11/3/06 PDF FILE	edeately following the v	UNIVERSITY OF HAWAII Aloha Observatory Engineering Support Facility 2525 Correa Road Honolulu, H196822